

Fig. 1

FIG. 2 is a block diagram of a network connection device 12. The device 12 includes three 10 base T interfaces 24, a virtual machine 10, and three virtual interfaces (egress) 26. The device 12 also includes a rules policy MIB 18 and a personality module. The device 12 is connected to three 10 base T networks and an ATM/ADSL network.

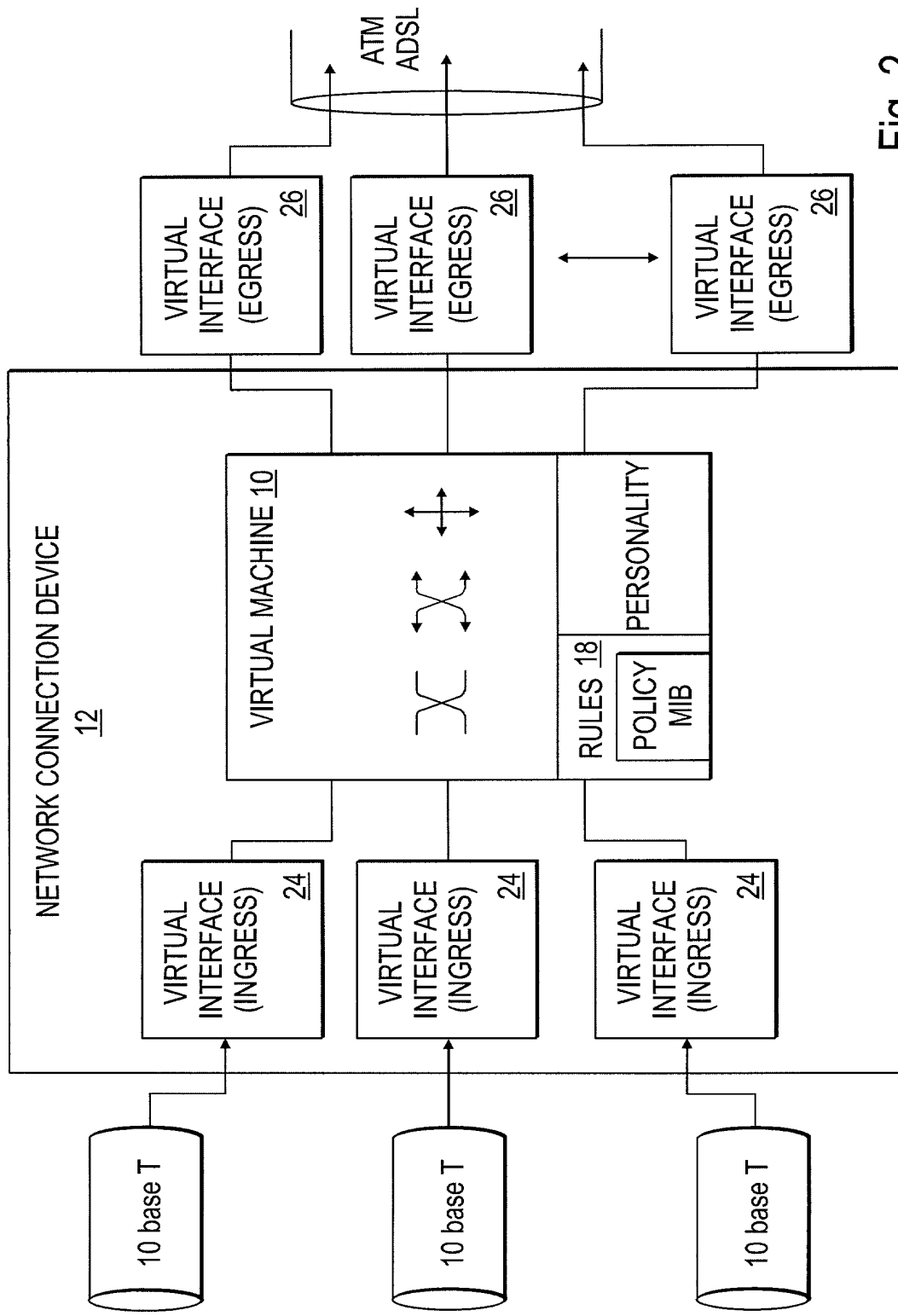


Fig. 2

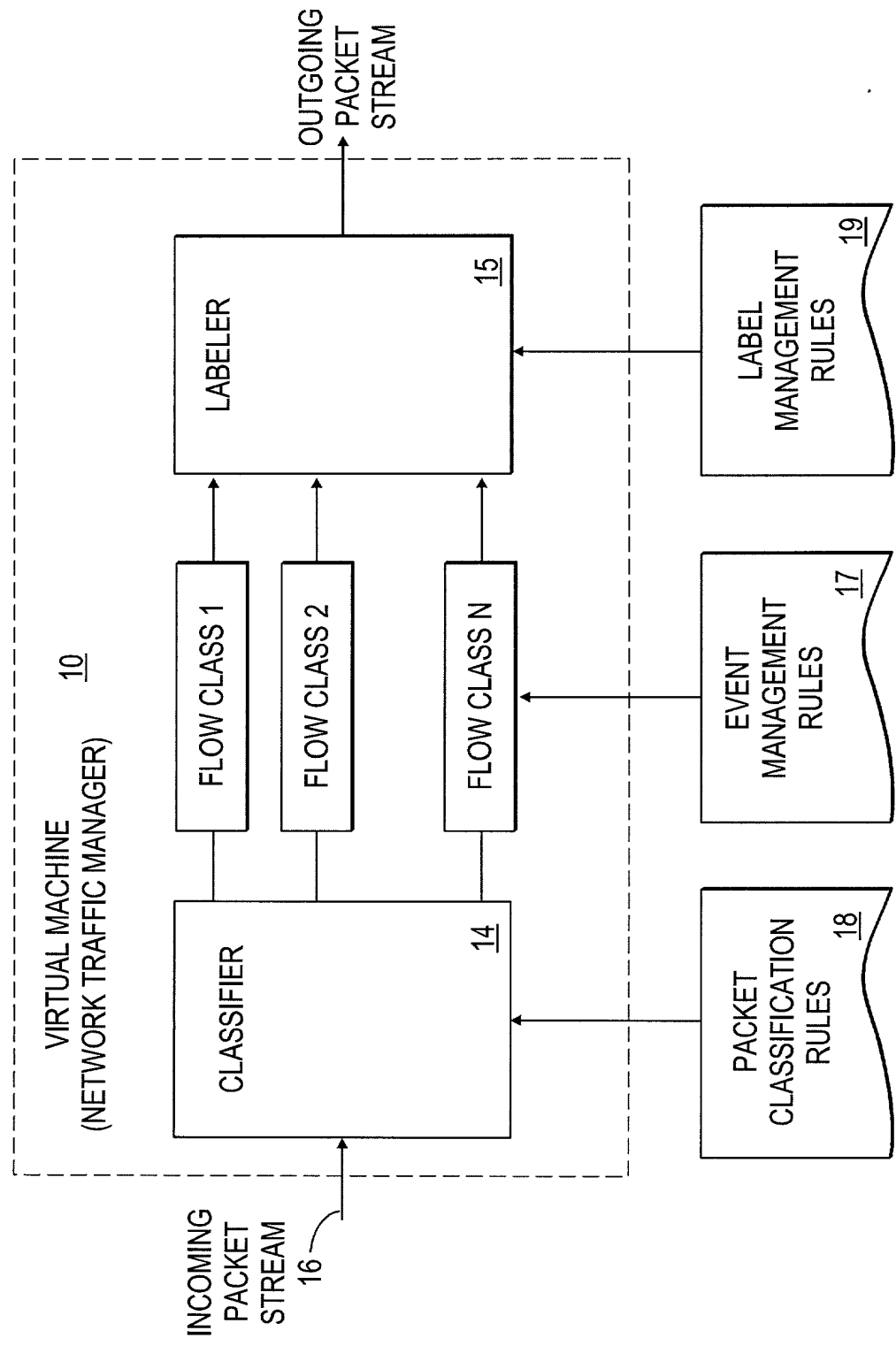


Fig. 3

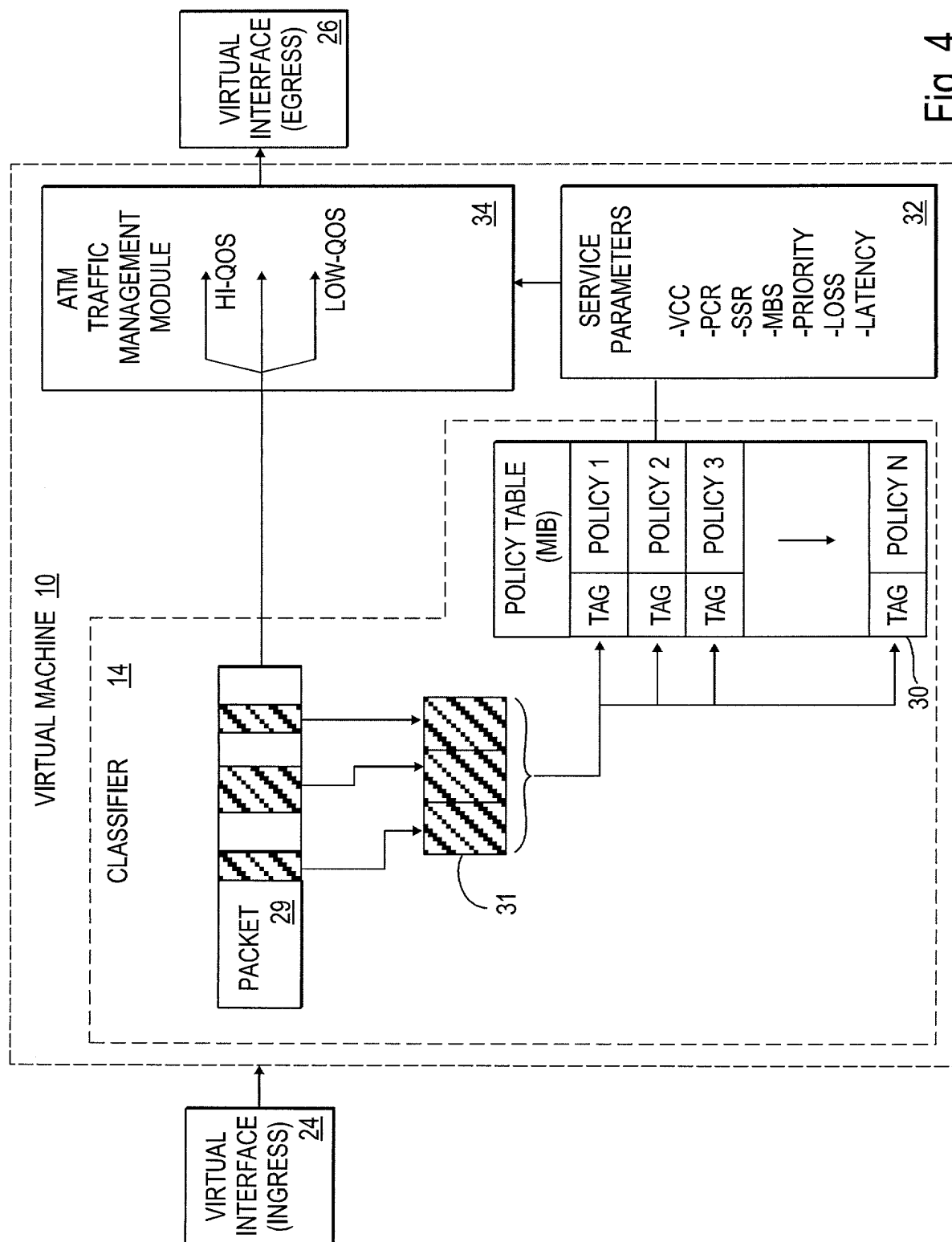


FIG. 5 is a block diagram of a system 30 for classifying network flows. The system 30 includes a policy table 30 and a flow class table 36. The policy table 30 includes a first column of flow class identifiers (FCD 1, FCD 2, FCD 3, ..., FCD N) and a second column of flow class names (FLOW CLASS 1, FLOW CLASS 1, FLOW CLASS 2, ..., FLOW CLASS 2). The flow class table 36 includes a first column of flow class names (FLOW CLASS 1, FLOW CLASS 2, FLOW CLASS 3, FLOW CLASS 4). Arrows indicate that FCD 1 maps to FLOW CLASS 1, FCD 2 maps to FLOW CLASS 1, FCD 3 maps to FLOW CLASS 2, and FCD N maps to FLOW CLASS 2. Additionally, FLOW CLASS 1 maps to FLOW CLASS 1 in the flow class table 36, FLOW CLASS 2 maps to FLOW CLASS 2 in the flow class table 36, and FLOW CLASS 2 maps to FLOW CLASS 4 in the flow class table 36.

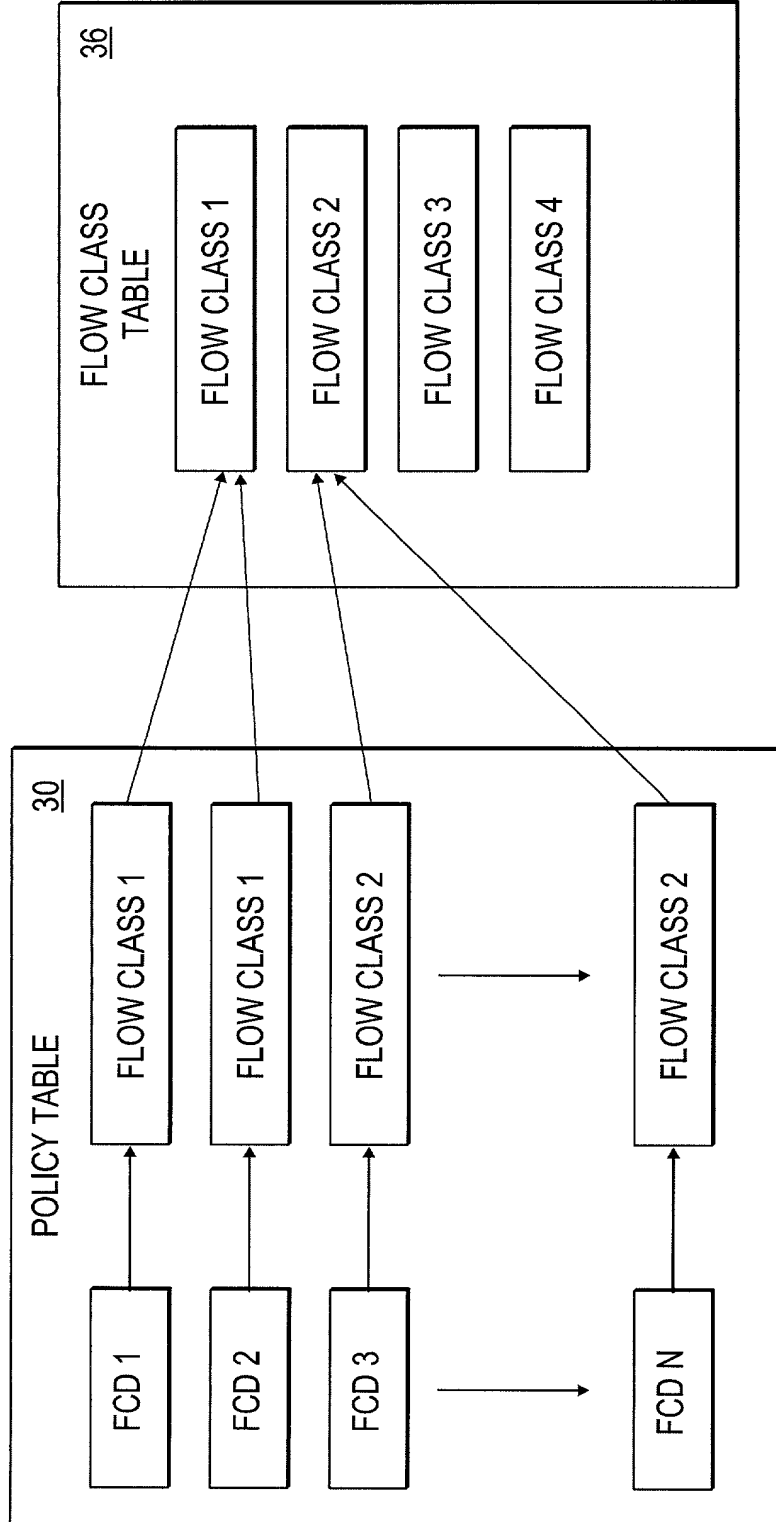


Fig. 5

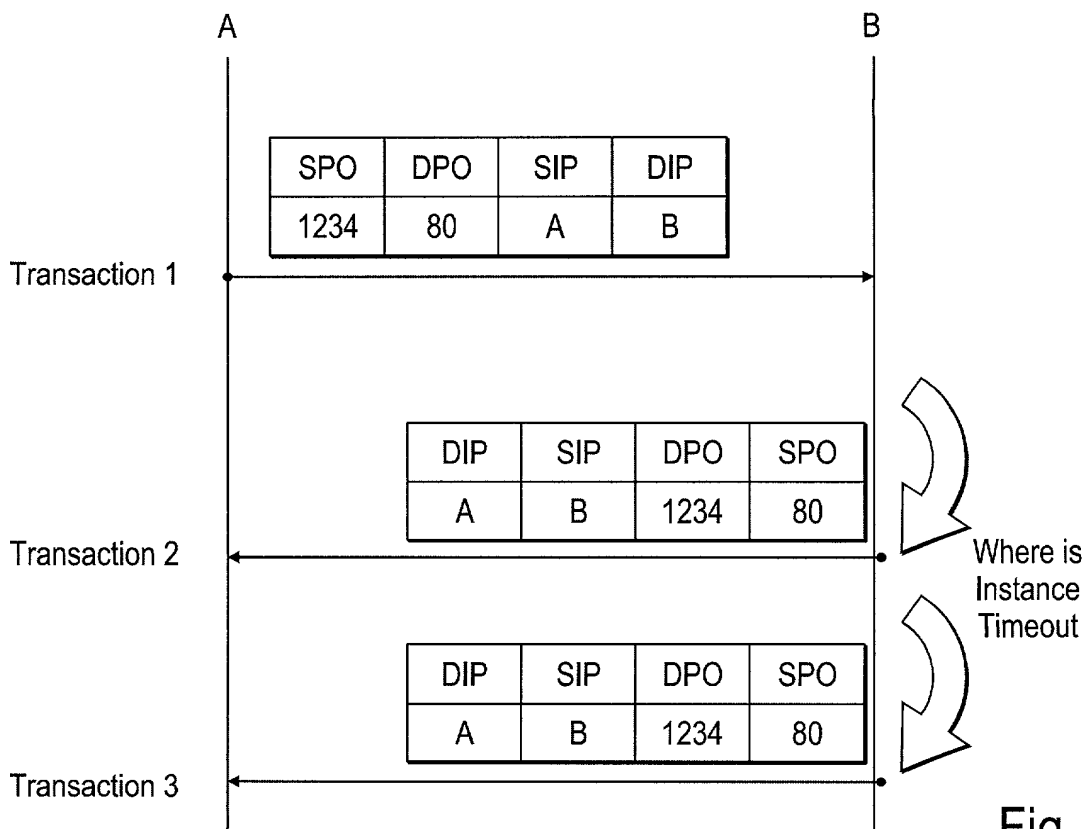


Fig. 6

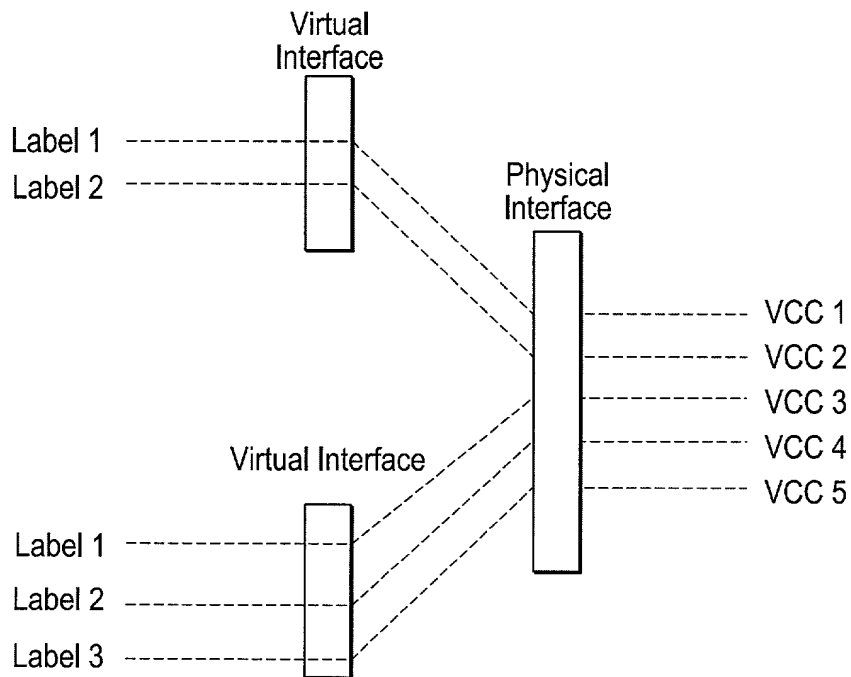


Fig. 7

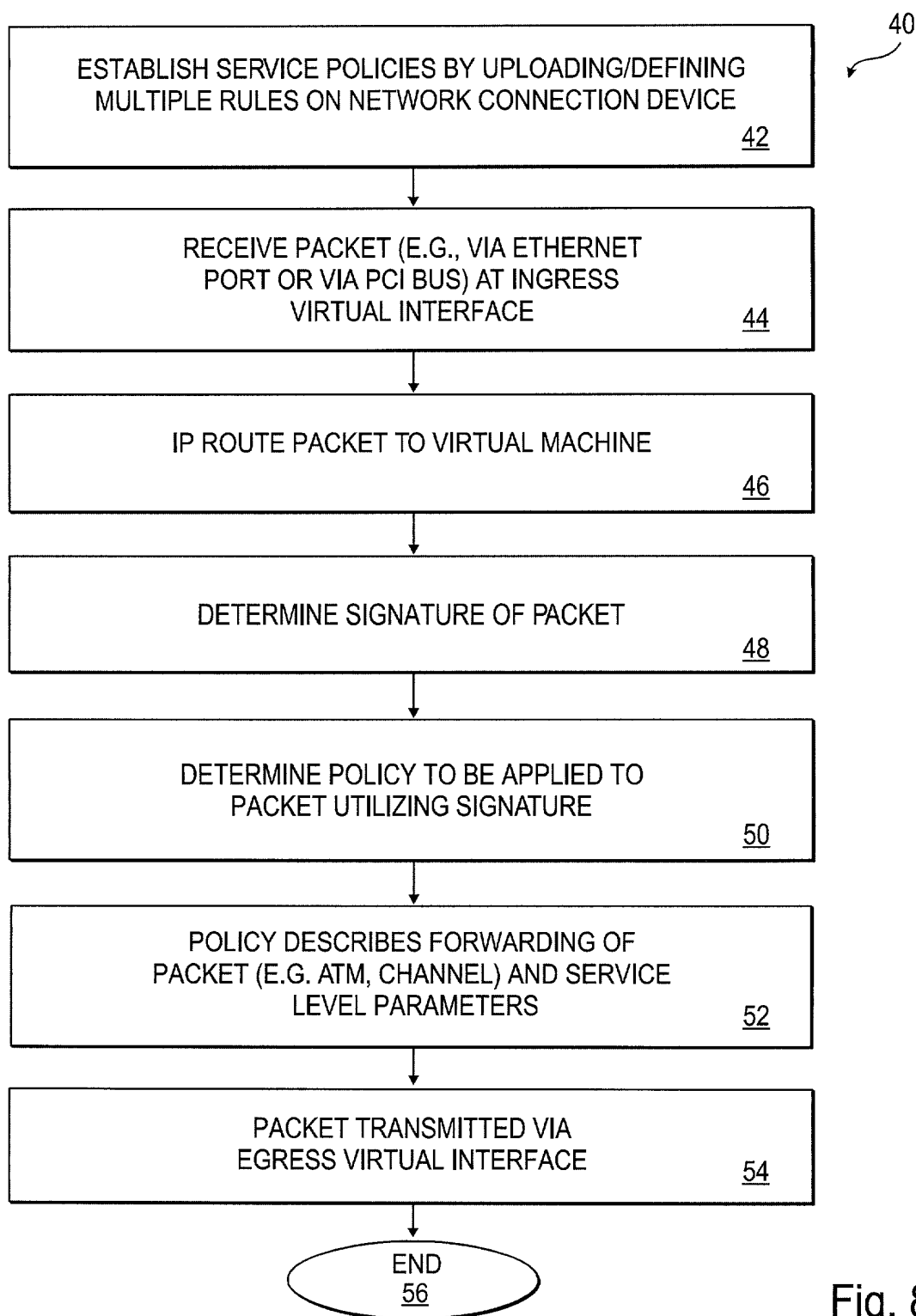


Fig. 8

FIG. 9 is a block diagram of a system for generating a virtual machine program. The system includes an operations file 62, a rule file 64, a virtual machine compiler 60, and a rule program (binary object) 66. The operations file 62 and the rule file 64 are inputs to the virtual machine compiler 60. The virtual machine compiler 60 outputs the rule program (binary object) 66, which is then used by the virtual machine.

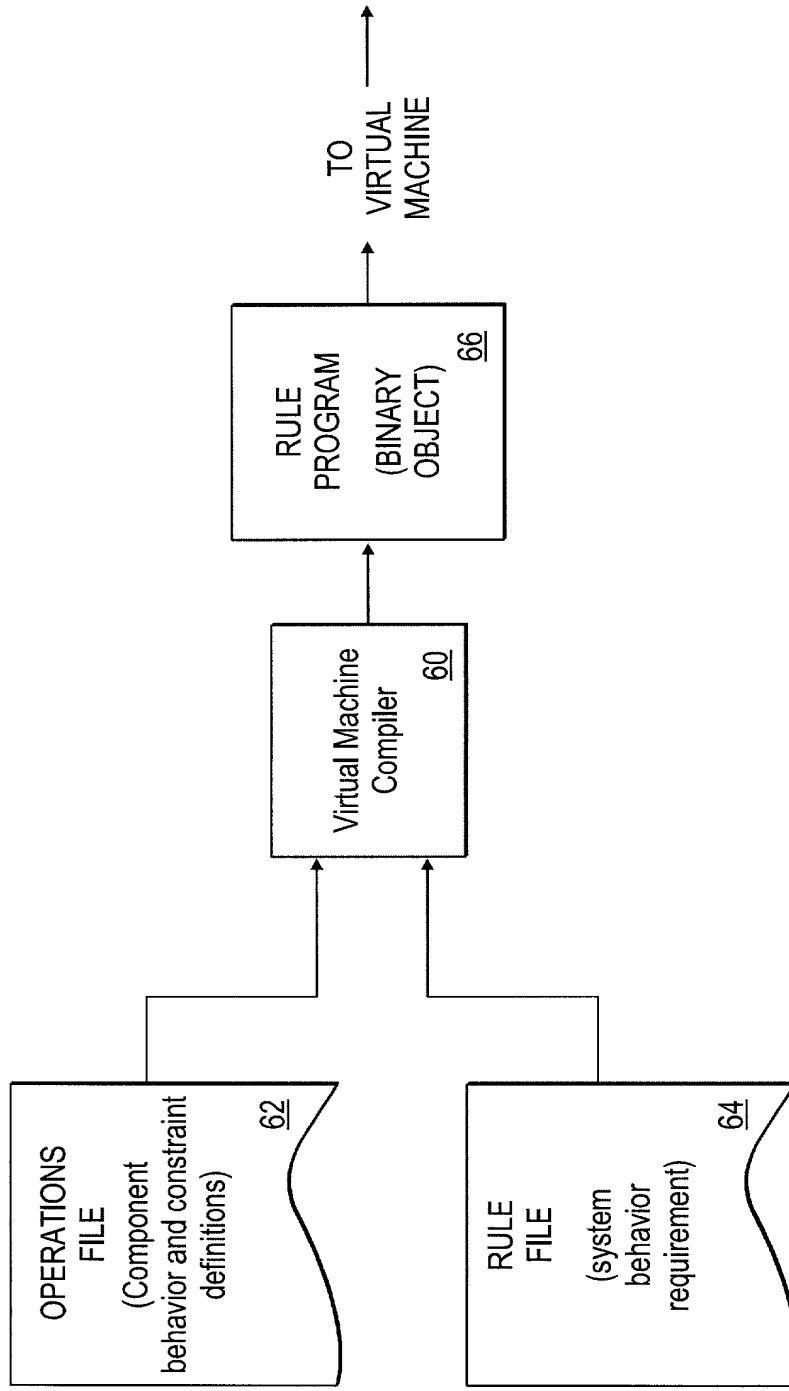


Fig. 9

US 2002/0102000 A1

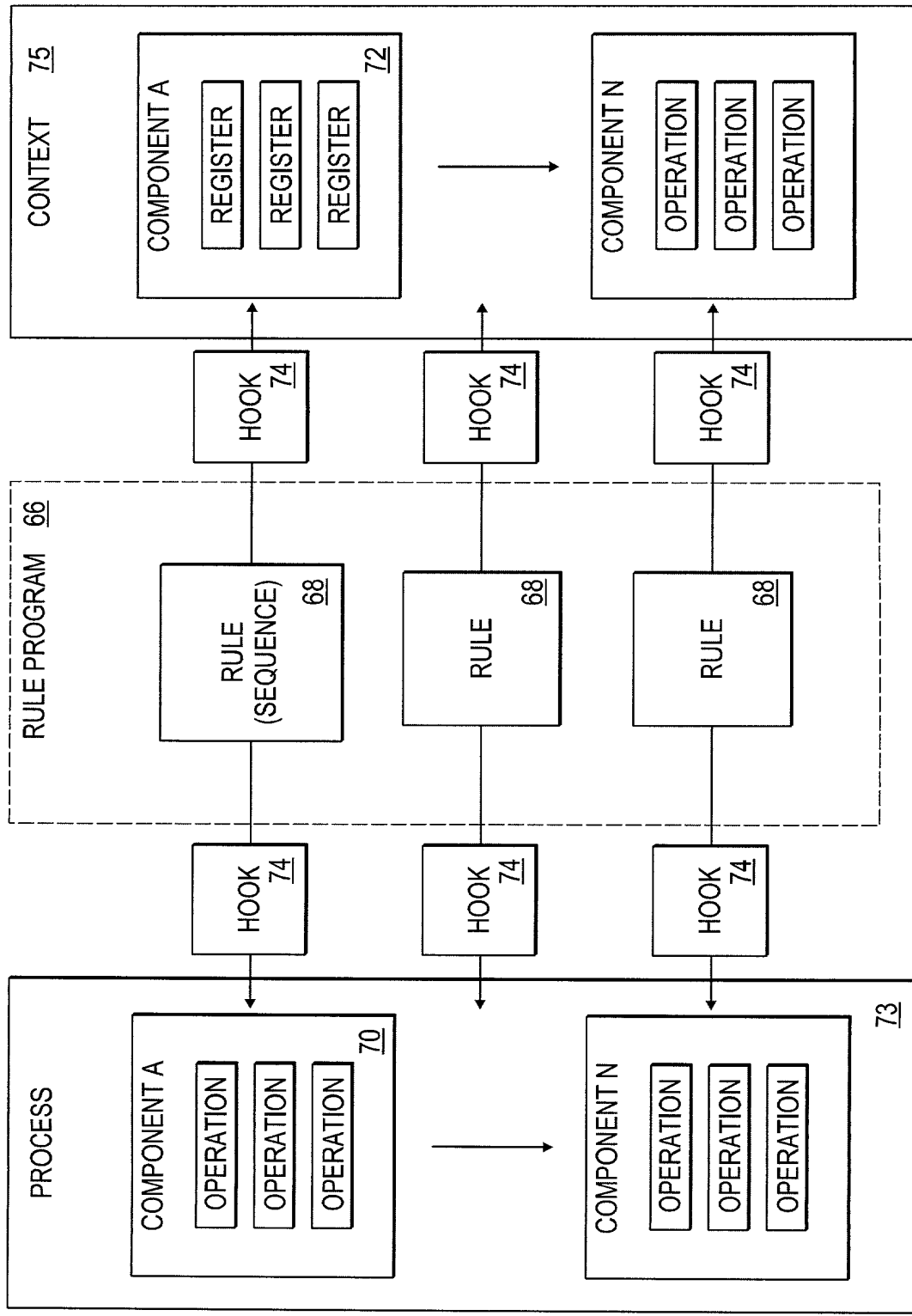


Fig. 10

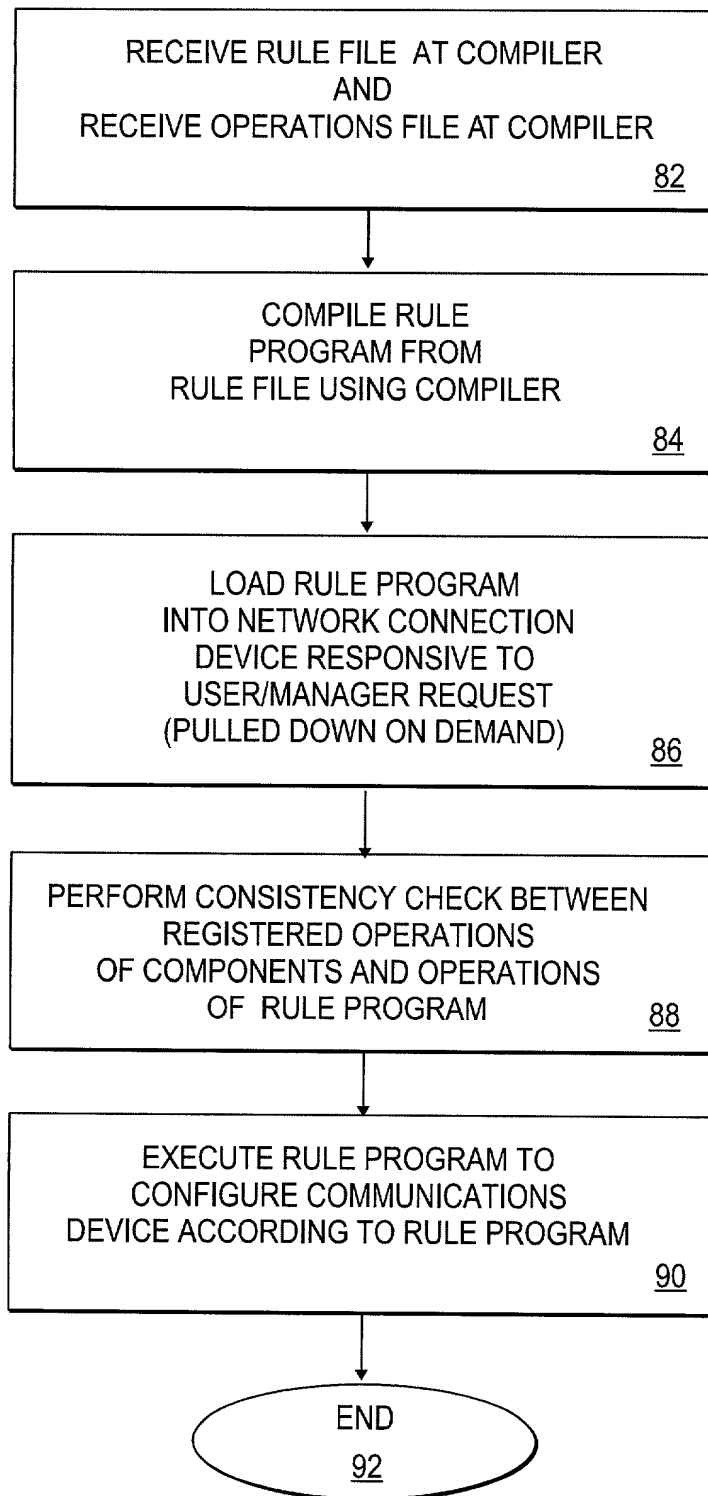


Fig. 11

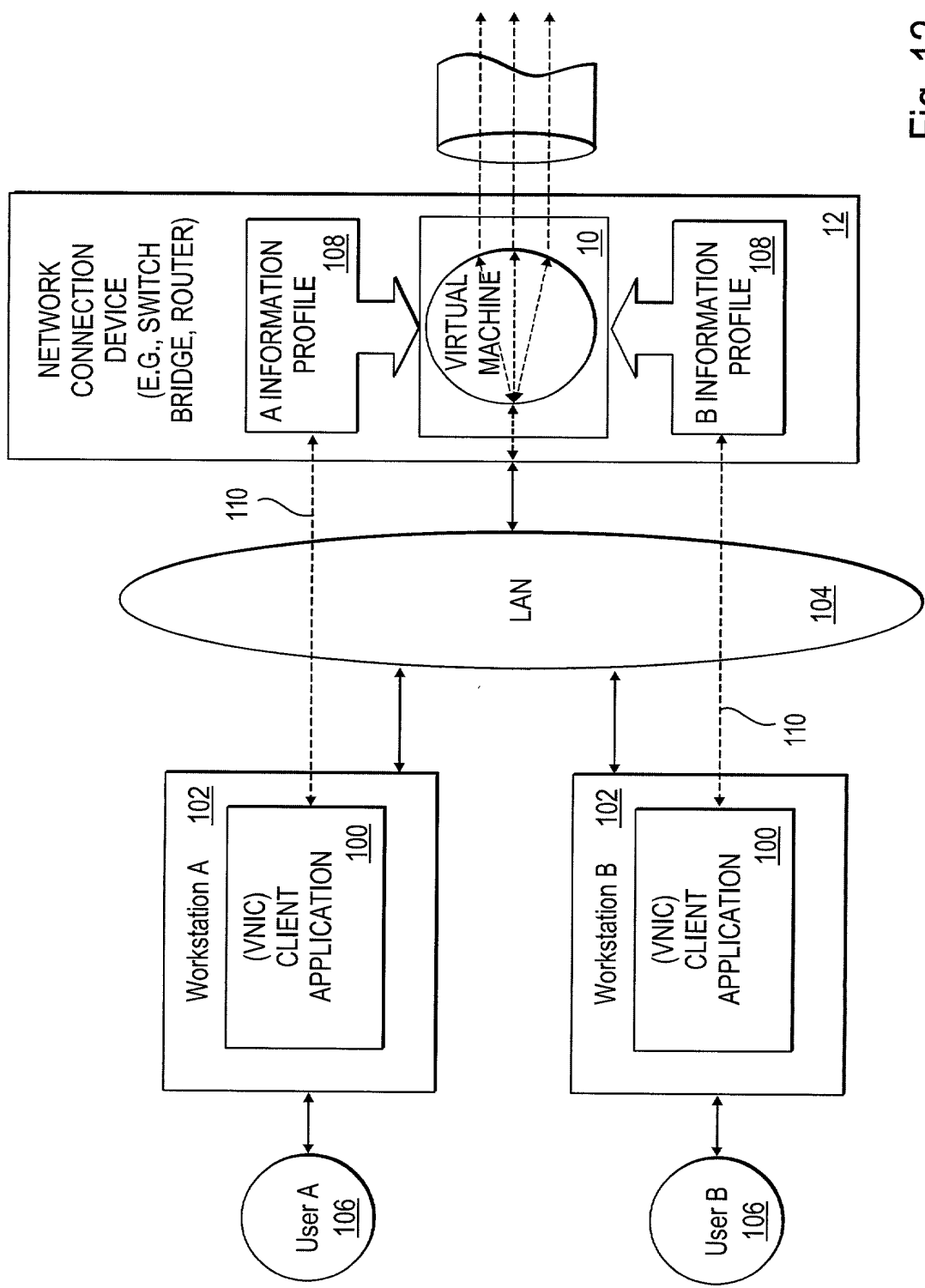


Fig. 12

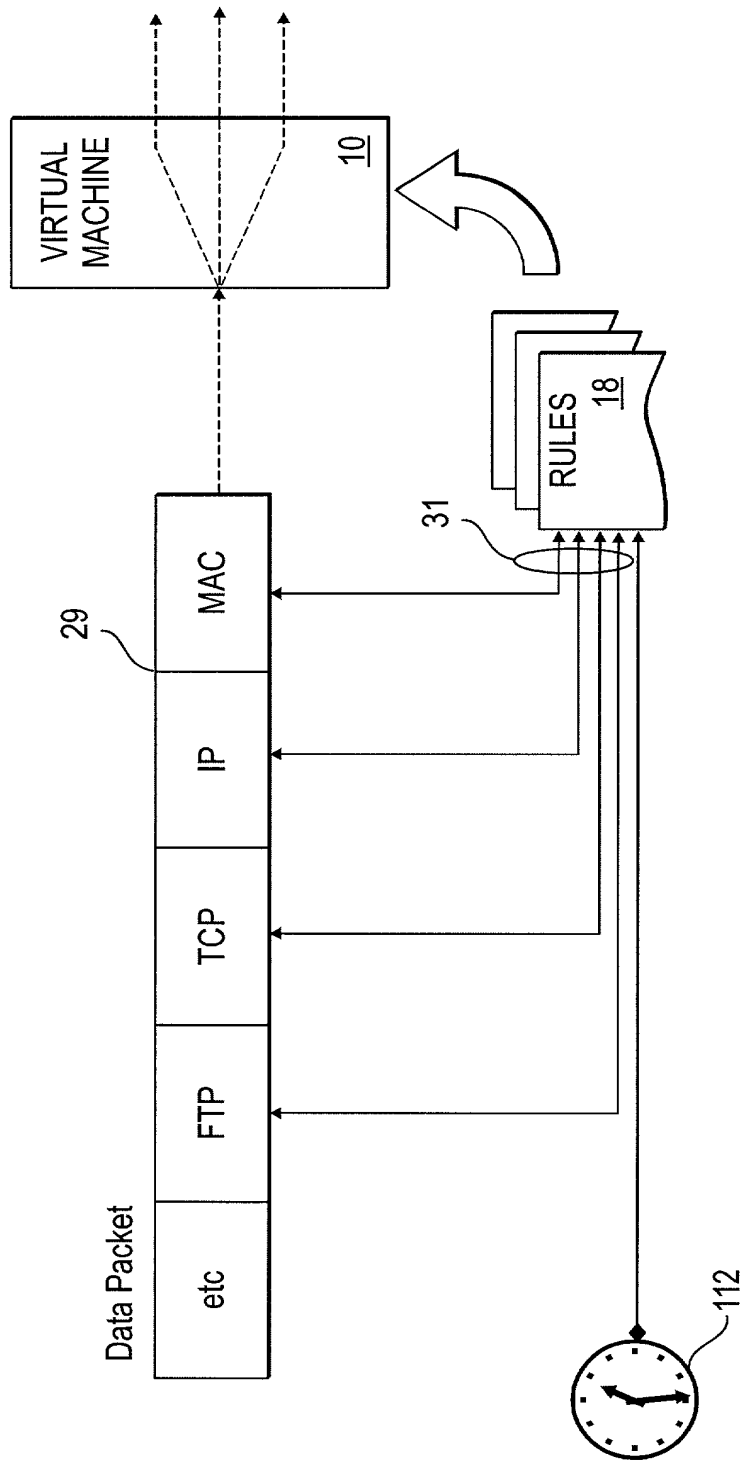


Fig. 13

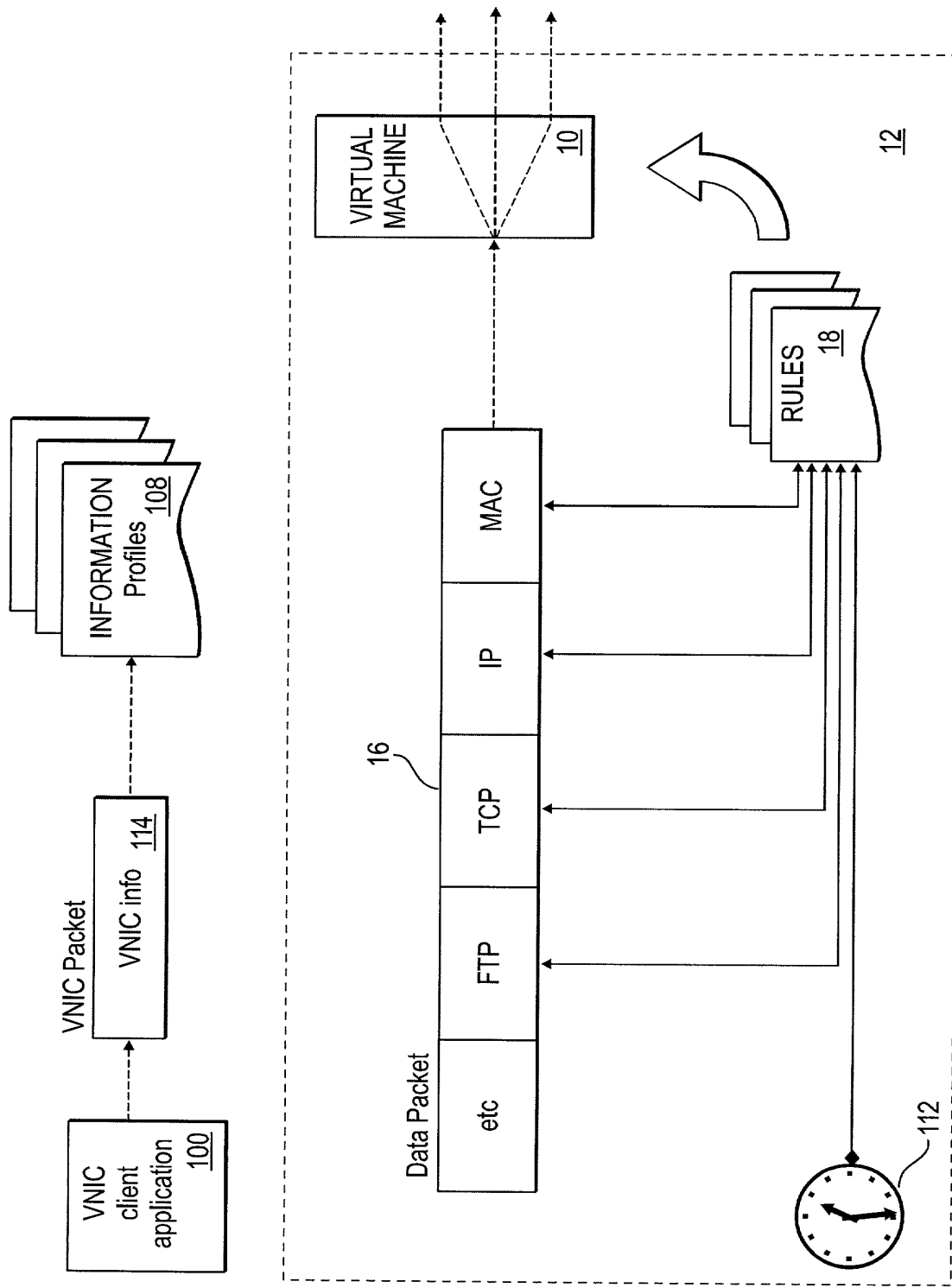


Fig. 14

US 2015/0100000 A1
2015.04.02
US 2015/0100000 A1
2015.04.02

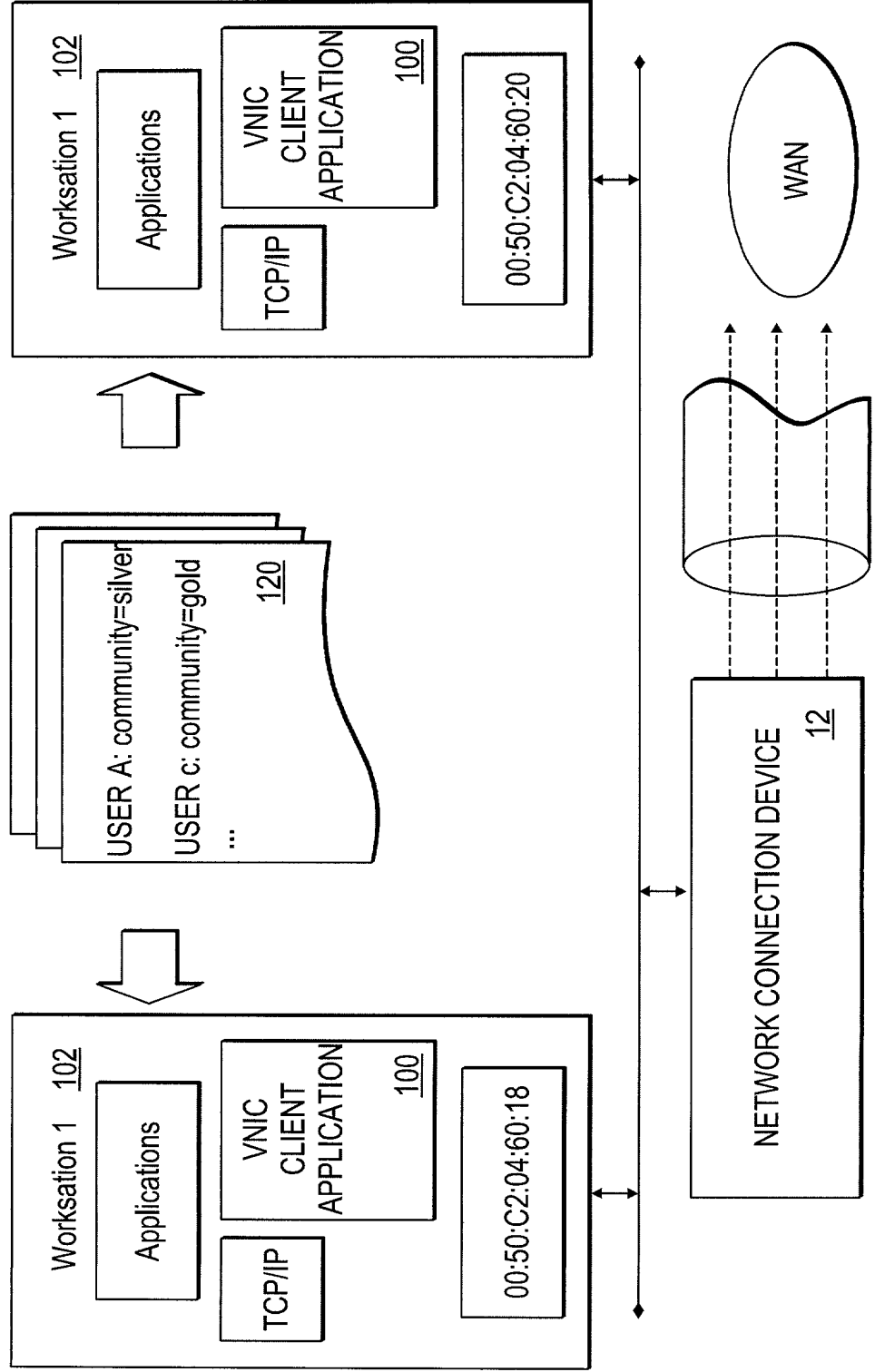


Fig. 15

FIG. 16 is a block diagram of a system architecture for bandwidth partitioning. The diagram shows a flow from MAC addresses to a data structure, then to a virtual machine, and finally to bandwidth partitions.

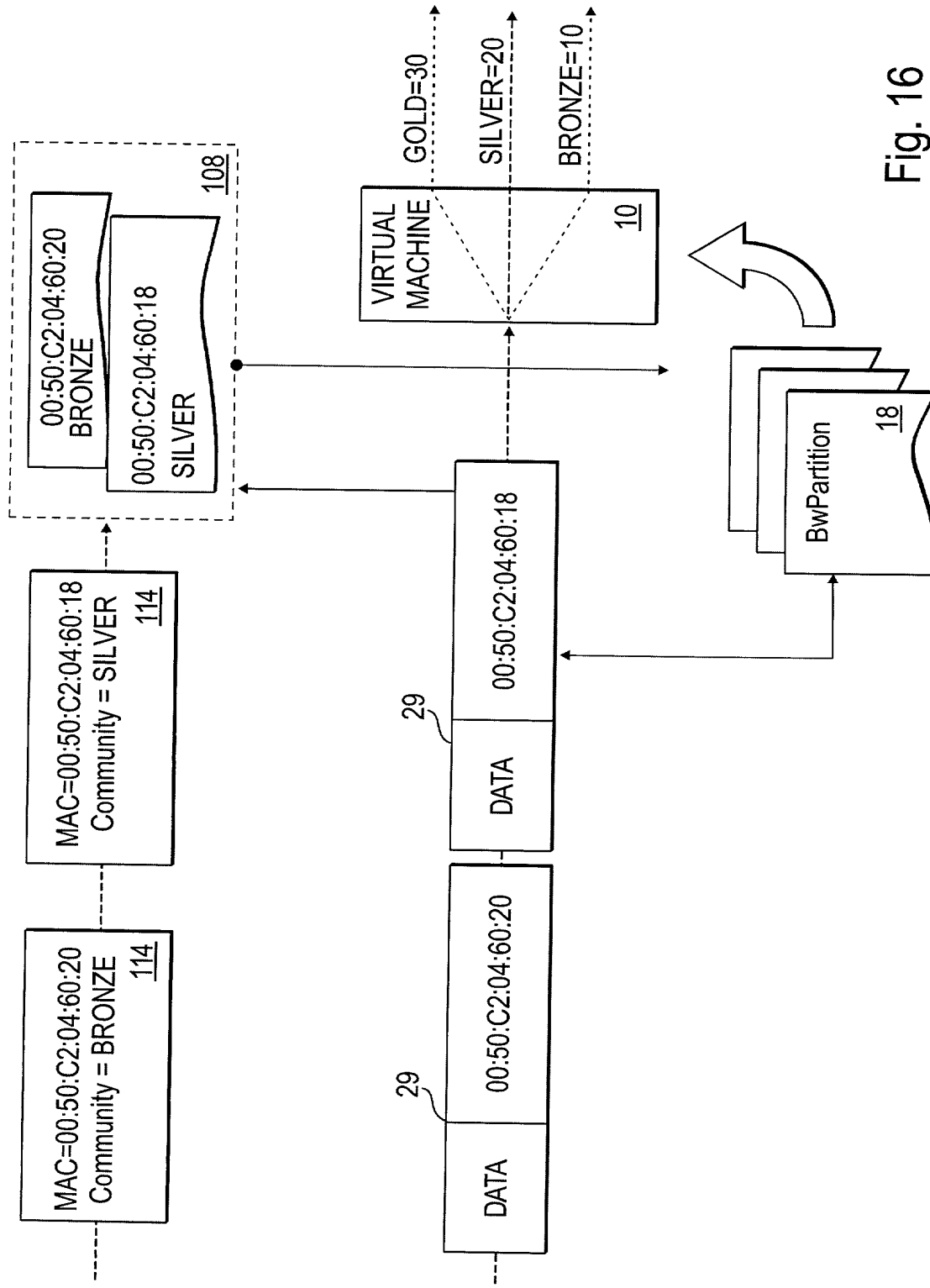


Fig. 16

FIG. 17 is a block diagram of a computer system 200. The system includes a processor 202, main memory 204, static memory 206, and a network interface device 220. The processor 202, main memory 204, and static memory 206 each contain instructions 226. The network interface device 220 is connected to a network. The system also includes a video display 210, an alpha-numeric input device 212, a cursor control device 214, a drive unit 216, and a signal generation device 218. The drive unit 216 contains a machine-readable medium 224 with instructions 226. All components are connected to a central bus 203.

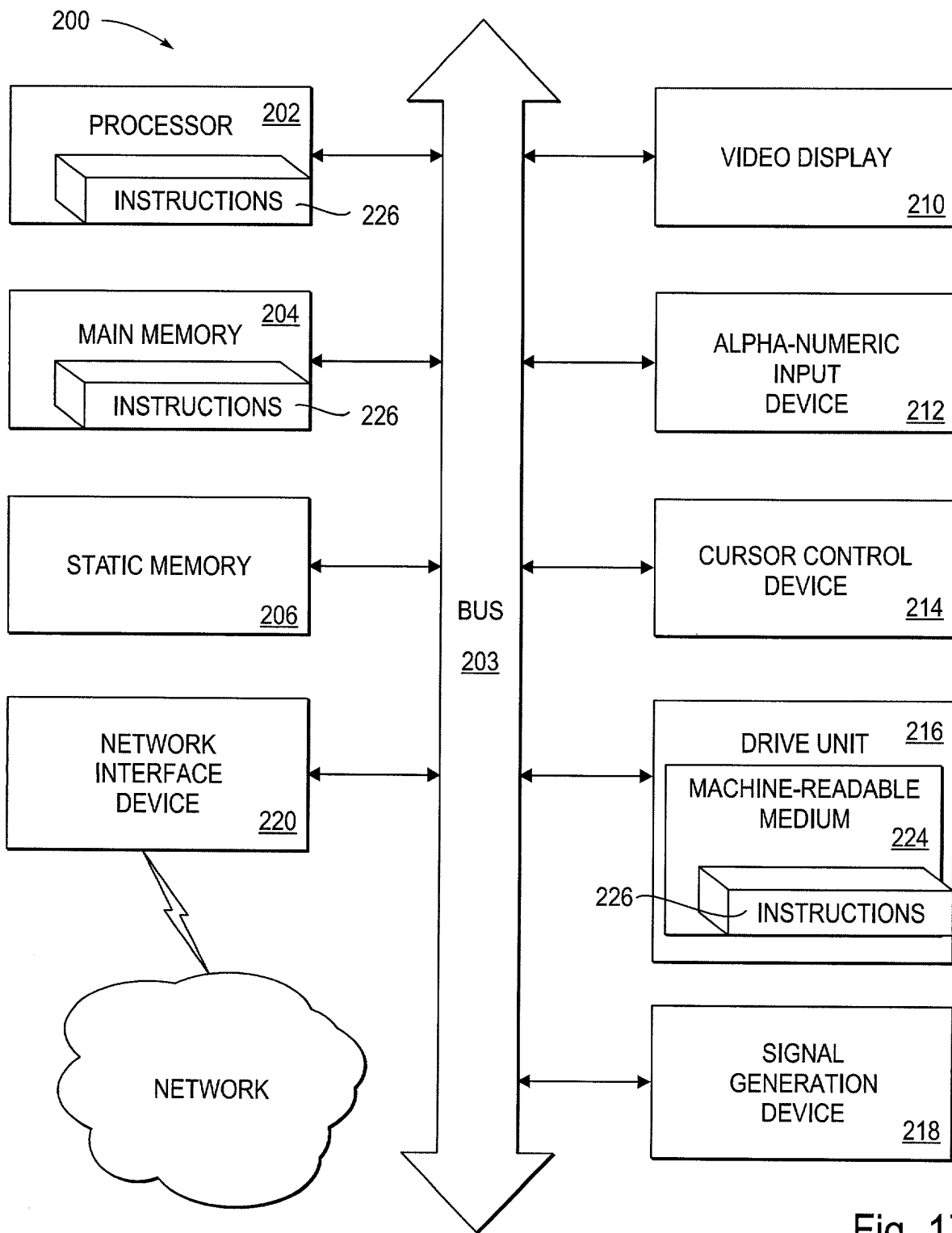


Fig. 17